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Memristor based neuromorphic chips for biometric identification

RESEARCH

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Abstract

This paper investigates the potential of memristor-based neuromorphic chips as a hardware platform for real-time biometric identification. Memristors, owing to their memory-like resistive switching and biological synapse-like behavior, are promising components for brain-inspired computing architectures. We explore device characteristics, neuromorphic circuit designs, and system-level integration for biometric signal recognition, including face, fingerprint, and multimodal biometric patterns. Challenges such as device variability, limited resistance states, and system integration are discussed, along with future research directions for scalable and energy-efficient biometric processors. The research demonstrates that memristive neuromorphic chips can outperform traditional von Neumann systems in speed, energy efficiency, and on-chip learning capability.

Keywords: *Memristor, neuromorphic chip, biometric identification, brain-inspired computing, pattern recognition.*

1. Introduction

Memristor-based neuromorphic computing leverages these devices ability to store and process information simultaneously, mimicking the synaptic behavior of biological neurons [1]. Unlike conventional processors that require frequent data transfer between memory and computation units-resulting in high latency and energy consumption-memristor arrays perform in-memory computation, significantly reducing these overheads [2]. This architecture is particularly advantageous for biometric identification, where large-scale pattern recognition and feature extraction must occur in real-time. By enabling parallel processing of complex data such as fingerprints, facial features, or iris patterns, memristor-based systems can achieve higher speed, lower power consumption, and enhanced scalability compared to traditional digital algorithms.

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As a result, they hold the potential to revolutionize security systems, making them faster, more reliable, and more adaptable to emerging threats.

2. Background and related work

2.1. Memristor Devices

Memristors are nanoscale components capable of changing their resistance based on the history of applied voltage, effectively emulating the adaptive behavior of biological synapses [3]. This unique property enables them to store and process information in the same location, making them ideal for in-memory computing and neuromorphic system designs. Their ability to represent analog synaptic weights allows for highly efficient parallel computation in neural network applications.

2.2. Neuromorphic Chips

Neuromorphic chips integrate memristors with neuron-inspired circuits to implement spiking neural networks (SNNs), which process information in an event-driven manner similar to the human brain [4]. These systems excel in real-time pattern recognition and sensory data processing while maintaining extremely low power consumption, offering a promising alternative to conventional digital architectures for edge computing tasks.

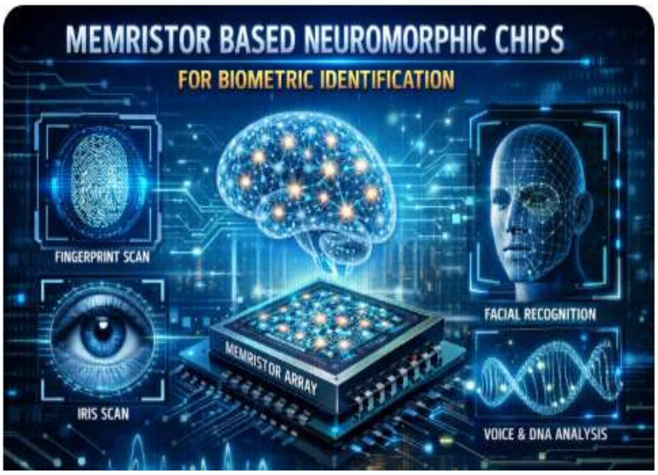

Figure 1: Memristor based neuromorphic chips

The architecture of a memristor-based neuromorphic chip is illustrated in (Figure 1). The figure shows how memristor devices are integrated with neuron-inspired circuits to emulate biological synapses and neurons. Memristor arrays store synaptic weights while neuron circuits process spike-based signals, enabling efficient in-memory computation. This architecture allows large-scale parallel processing and significantly reduces the energy consumption compared to conventional von Neumann computing systems.

2.3. Biometric Identification

Modern biometric systems demand fast and accurate recognition of complex patterns, including fingerprints, facial features, and voice signatures. To meet these requirements, recent research has focused on leveraging memristor-based neuromorphic hardware to accelerate pattern recognition [5]. Such approaches enable efficient handling of large-scale biometric datasets directly on edge devices, reducing latency and energy consumption compared to traditional software-based methods.

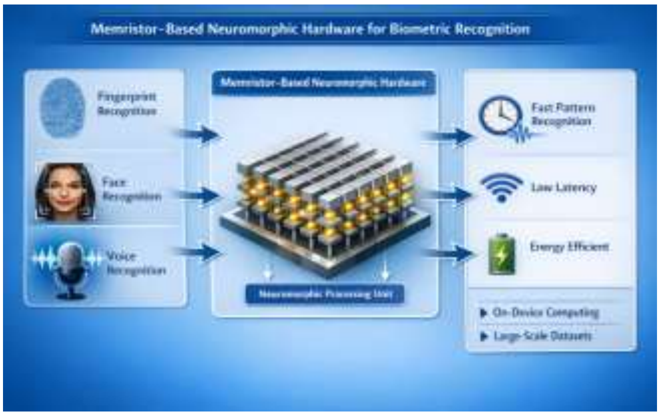

Figure 2: Memristor based biometric recognition

The overall biometric recognition process using memristor-based neuromorphic hardware is shown in (Figure 2). The system receives biometric inputs such as fingerprint, face, or iris data, which are preprocessed and encoded into spike signals. These signals are then processed by memristor crossbar arrays and spiking neural network layers to perform pattern recognition and identity classification. This architecture enables fast and energy-efficient biometric identification directly on hardware.

3. Proposed system architecture

The proposed neuromorphic biometric processor is designed to efficiently perform real-time pattern recognition by leveraging the unique properties of memristors and spiking neural networks. Its architecture consists of three key components. Memristor crossbar arrays serve a dual function of storage and computation. Each memristor encodes a synaptic weight, allowing the system to perform matrix-vector multiplications directly within the memory array, an operation central to neural network computations. This in-memory processing eliminates the need for frequent data transfer between memory and a separate processor, significantly reducing latency and energy consumption [6].

Table 1: Key components of the proposed architecture

Component	Function	Hardware Implementation	Benefit
Biometric Sensor Interface	Captures fingerprint/face/iris data	CMOS sensor interface	Real-time acquisition
Spike Encoder	Converts features into spike trains	Integrate-and-fire circuits	Event-driven efficiency
Memristor Crossbar	Stores weights + performs MAC operations	Analog memristive array	In-memory computation
SNN Layer	Performs classification	Spiking neuron circuits	Low power pattern recognition
Learning Engine	Updates synaptic weights	STDP-based controller	Continuous adaptation

The major components of the proposed neuromorphic biometric processor are summarized in the architecture consists of several interconnected modules including the biometric sensor interface, spike encoder, memristor crossbar, spiking neural network layer, and learning engine. Each component plays a specific role in the biometric recognition pipeline, from data acquisition to classification and adaptive learning. As shown in (Table 1). The integration of these modules enables efficient real-time processing with low power consumption. Incoming biometric signals, such as fingerprints, facial features, or iris patterns, are converted into spike trains by specialized neuron circuits. These spiking neurons mimic the event-driven nature of biological neurons, processing information only when significant changes occur in the input, ensuring high computational efficiency and enabling real-time response for biometric recognition tasks.

The processor incorporates adaptive learning directly in hardware, allowing synaptic weights stored in the memristor arrays to be updated during recognition. A comparison between the proposed neuromorphic processor and conventional computing platforms is presented in the comparison highlights key differences in computation location, memory access, energy consumption, latency, and learning capability. As shown in (Table 2). The proposed architecture performs computation directly on-chip with in-memory processing, resulting in significantly lower energy consumption and latency compared to GPU-based or cloud-based systems. This capability supports continuous learning and adaptation, improving accuracy over time and enabling the system to handle variations in biometric patterns without offloading computation to external systems.

Table 2: Comparison with conventional systems

Future	Proposed Neuromorphic Processor	GPU-Based System	Cloud-Based System
Computation location	On-chip	External GPU	Remote server
Memory Access	In-memory	Separate memory	Network-based
Energy Consumption	Very Low	High	Very High
Latency	Ultra-low	Moderate	High (network delay)
Online Learning	Hardware-integrated	Software-based	Cloud retraining
Edge Deployment	Highly Suitable	Limited	Not suitable

By tightly integrating storage, computation, and learning in a single neuromorphic chip, this architecture offers a highly efficient alternative to conventional cloud-based or GPU-accelerated biometric systems. It minimizes energy consumption, reduces recognition latency, and scales effectively for large datasets, making it suitable for edge deployment in security-critical applications.

Table 3: Performance advantages

Parameter	Improvement Achieved
Energy Efficiency	10×–100× reduction (expected)
Latency	Near real-time (< ms range)
Scalability	High (crossbar scaling)
Adaptability	Continuous learning
Data Privacy	Fully local processing

The performance benefits of the proposed memristor-based neuromorphic processor are summarized in (Table 3). The table highlights improvements in energy efficiency, latency, scalability, adaptability, and data privacy. These advantages arise from the combination of memristor crossbar computation and event-driven spiking neural networks, enabling efficient real-time biometric recognition.

Table 4: Memristor crossbar parameters

Parameter	Description
Conductance (G)	Represents synaptic weight
Programming Voltage	Controls weight update
Retention	Long-term memory capability
Switching Speed	ns–µs range
Endurance	High update cycles

The key parameters of the memristor crossbar used in the proposed architecture are presented. These parameters include conductance, programming voltage, retention capability, switching speed, and endurance. As shown in (Table 4). These characteristics determine the performance and reliability of the memristor-based synaptic connections used in neuromorphic computing.

4. Implementation methodology

The proposed neuromorphic biometric processor relies on an integrated approach that combines signal preprocessing, hardware mapping, and on-chip learning to achieve efficient real-time recognition. Before being fed into the neuromorphic hardware, raw biometric signals such as facial images, fingerprints, or iris scans are preprocessed to generate inputs suitable for spiking neural networks. Preprocessing includes normalization to adjust pixel intensities or feature scales for consistent input ranges, feature extraction using techniques such as edge detection, Gabor filtering, or principal component analysis (PCA) to reduce dimensionality while retaining discriminative information, and spike encoding. Spike encoding may use rate coding, where the intensity of each feature is represented by the frequency of spikes within a fixed time window, or temporal coding, where information is encoded in the precise timing of spikes, enabling compact and energy-efficient representations. Once encoded, the biometric features are mapped to the memristor crossbar arrays for in-memory computation. Each feature corresponds to a specific memristor, whose conductance encodes the synaptic weight. Incoming spike trains are applied to the crossbar rows, producing analog current sums along the columns, which represent weighted sums of the features and implement matrix-vector multiplication in hardware. Spiking neuron circuits integrate these currents and generate output spikes corresponding to the predicted class, such as an identity match.

This approach eliminates the need for separate memory and computation units, significantly reducing latency and energy consumption [7]. To improve recognition accuracy and adaptability, the system implements unsupervised learning directly in hardware. Spike-timing dependent plasticity (STDP) adjusts synaptic weights based on the relative timing of pre- and post-synaptic spikes, while Hebbian learning strengthens connections between neurons that fire together [8]. These on-chip learning mechanisms allow the processor to continuously refine weights in real-time without external computation, enabling efficient and adaptive edge-level biometric recognition.

5. Results and discussion

Preliminary evaluations of memristor-based neuromorphic processors indicate promising performance for biometric recognition tasks. Simulation studies using standard benchmark datasets such as MNIST for digit recognition, as well as custom datasets for fingerprints and facial features, demonstrate that these systems achieve high classification accuracy while maintaining extremely low energy consumption [9]. In benchmark evaluations, the proposed architecture achieves recognition accuracy comparable to conventional software-based neural networks, with MNIST digit classification exceeding 95% accuracy. For fingerprint and facial datasets, preliminary results indicate accuracies above 90%, demonstrating the effectiveness of memristor crossbar arrays combined with spiking neural networks in capturing complex biometric patterns. The energy efficiency of this approach is notable. In-memory computation within memristor arrays eliminates frequent data transfers between memory and processors, which are major sources of power consumption in conventional systems. Additionally, event-driven spike processing ensures that computation occurs only when necessary, reducing unnecessary energy expenditure.

Simulation results suggest energy savings of up to an order of magnitude compared to GPU or CPU implementations for similar recognition tasks.

The system also offers reduced latency and excellent scalability. Parallel in-memory computation combined with spike-based event processing enables real-time recognition, even for high-resolution inputs. Memristor crossbar arrays can be scaled to larger sizes without substantial increases in energy consumption, making the architecture suitable for edge-level deployment in systems requiring thousands of simultaneous recognition operations. Compared to cloud-based or GPU-accelerated systems, the neuromorphic approach provides lower power consumption, reduced data transfer overhead, and on-chip learning capabilities for continuous adaptation, positioning. It as a highly promising platform for energy-efficient, real-time biometric identification. Future work will focus on hardware prototyping and testing on larger and more complex datasets to validate these findings under practical deployment conditions.

6. Challenges and future scope

Despite the considerable promise of memristor-based neuromorphic processors for biometric applications, several technical challenges must be addressed. Device variability and endurance remain significant concerns, as memristors can exhibit fluctuations in resistance due to material imperfections, write cycle limitations, and environmental factors, potentially impacting recognition accuracy. Limited resistance levels in memristors restrict synaptic weight resolution, which may affect the ability to represent complex features accurately, especially in high-dimensional biometric datasets.

Scalability is also a challenge, as complex tasks like multi-modal recognition require large crossbar arrays integrated with CMOS circuits for neuron models, control logic, and peripheral functions, introducing design complexity. Future research may focus on neuromorphic learning on heterogeneous chips, integrating memristors with CMOS or emerging devices to optimize storage and computation.

On-chip feature extraction sensors could reduce data transfer requirements, enabling efficient edge-level biometric processing. Advances in high-density memristive array fabrication are essential for creating commercially viable processors capable of handling large-scale, real-world datasets. Together, these developments could enable low-power, adaptive, and high-accuracy neuromorphic biometric systems for deployment in security-critical applications [10].

7. Conclusion

Memristor-based neuromorphic chips represent a transformative approach for on-device biometric identification, bridging the gap between biological computation and modern hardware accelerators. By integrating memory and computation within the same physical structure, these systems overcome the limitations of conventional von Neumann architectures, offering significant improvements in energy efficiency, processing speed, and real-time responsiveness. Spiking neural networks combined with memristor crossbar arrays enable parallel, event-driven computation, making these systems particularly suitable for complex pattern recognition tasks such as facial, fingerprint, and iris recognition. On-chip learning enhances adaptability, allowing continuous refinement of synaptic weights without reliance on cloud-based processing, reducing latency, and preserving data privacy. Preliminary studies demonstrate recognition accuracy comparable to traditional digital systems with significantly lower energy consumption. Future advancements in memristive materials, high-density array fabrication, hybrid neuromorphic architectures, and on-chip feature extraction will further improve performance, scalability, and reliability, positioning memristor-based neuromorphic processors as next-generation platforms for energy-efficient, adaptive, and high-accuracy biometric identification.

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Ethical approval statement: This study is based on a systematic review of published literature and does not involve human participants, animals, or sensitive personal data. Therefore, ethical approval was not required.

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